IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A drive circuit ~~for a semiconductor device~~ for driving an insulated gate transistor, said drive circuit comprising:

a driver ~~for applying~~ configured to apply a gate voltage to said transistor; and

a timing controller ~~for controlling~~ configured to control a timing of said driver,

wherein said driver includes first and second drive circuits, said first and second drive circuits are electrically connected to said timing controller through first and second electrical connections, respectively, said first and second electrical connections control said first and second drive circuits, respectively, and said driver is capable of applying [[as]] said gate voltage as a first gate voltage through said first drive circuit to said transistor, and as a second gate voltage through said second drive circuit to said transistor, said first gate voltage being lower than a threshold voltage of said transistor, and said second gate voltage being a specified voltage for driving said transistor, and

wherein said timing controller [[so]] controls said driver so that an application of said first gate voltage precedes an application of said second gate voltage.

Claim 2 (Currently Amended): [[The]] A drive circuit ~~according to claim 1,~~ for driving an insulated gate transistor, said drive circuit comprising:

a driver for applying a gate voltage to said transistor; and

a timing controller for controlling a timing of said driver,

wherein said driver is capable of applying said gate voltage as a first gate voltage and as a second gate voltage to said transistor, said first gate voltage being lower than a threshold

voltage of said transistor, and said second gate voltage being a specified voltage for driving said transistor,

wherein said timing controller controls said driver so that an application of said first gate voltage precedes an application of said second gate voltage,

wherein said driver is capable of further applying [[as]] said gate voltage as a third gate voltage to said transistor, said third gate voltage being higher than said first gate voltage and lower than said second gate voltage, and

wherein said timing controller [[so]] controls said driver so that application of said third gate voltage follows application of said first gate voltage, and application of said second gate voltage follows a recovery current of a main current of said transistor within a mirror effect time of said transistor.

Claim 3 (Original): The driver circuit according to claim 2, further comprising:

a voltage supply unit for generating said third gate voltage on the basis of said main current, and supplying said third gate voltage to said driver.

Claim 4 (Currently Amended): The drive circuit according to claim 3,

wherein said voltage supply unit generates said third gate voltage on the basis of a predetermined function which involves said main current as a variable.

Claim 5 (Currently Amended): The drive circuit according to claim 3,

wherein said voltage supply unit generates said third gate voltage on the basis of said main current flowing in a period excluding turn-on and turn-off of said transistor.

Claim 6 (Currently Amended): The drive circuit according to claim 3,

wherein said voltage supply unit holds [[the]] a maximum value of said main current in a drive period of said transistor, to generate said third gate voltage on the basis of said maximum value to be applied in a subsequent drive period of said transistor.

Claim 7 (Currently Amended): The drive circuit according to claim 3,

wherein said voltage supply unit calculates [[the]] an average of said main current obtained from a plurality of drive periods of said transistor, to generate said third gate voltage on the basis of said average of said main current to be applied in a subsequent drive period of said transistor.

Claim 8 (Currently Amended): The drive circuit according to claim 3,

wherein said voltage supply unit generates said third gate voltage which increases as said main current increases.

Claim 9 (Currently Amended): The drive circuit according to claim 3,

wherein said voltage supply unit controls said third gate voltage to allow slowdown in switching speed of said transistor when said main current is lower than a predetermined level.

Claim 10 (Currently Amended): A drive circuit ~~for a semiconductor device~~ for driving an insulated gate transistor, said drive circuit comprising:

a voltage supply unit ~~for generating~~ configured to generate a gate voltage to be applied to said transistor on the basis of a main current of said transistor;

a driver ~~for applying~~ configured to apply said gate voltage generated by said voltage supply unit to said transistor, said driver including first, second, and third drive circuits, said first and second drive circuits being configured to apply first and second gate voltages to said transistor, and said third drive circuit being configured to apply said gate voltage, which is different from said first and second gate voltages; and

a timing controller ~~for controlling~~ configured to control a timing of application of said gate voltage by said driver.

Claim 11 (Original): The drive circuit according to claim 10,

wherein said voltage supply unit generates said gate voltage on the basis of a predetermined function which involves said main current as a variable.

Claim 12 (Original): The drive circuit according to claim 10,

wherein said voltage supply unit generates said gate voltage on the basis of said main current flowing in a period excluding turn-on and turn-off of said transistor.

Claim 13 (Currently Amended): The drive circuit according to claim 10,

wherein said voltage supply unit holds [[the]] a maximum value of said main current in a drive period of said transistor, to generate said gate voltage on the basis of said maximum value to be applied in a subsequent drive period of said transistor.

Claim 14 (Currently Amended): [[The]] A drive circuit ~~according to claim 10,~~ for driving an insulated gate transistor, said drive circuit comprising:

a voltage supply unit for generating a gate voltage to be applied to said transistor on the basis of a main current of said transistor;

a driver for applying said gate voltage generated by said voltage supply unit to said transistor; and

a timing controller for controlling a timing of an application of said gate voltage by said driver,

wherein said voltage supply unit calculates [[the]] an average of said main current obtained from a plurality of drive periods of said transistor, to generate said gate voltage on the basis of said average of said main current to be applied in a subsequent drive period of said transistor.

Claim 15 (Original): The drive circuit according to claim 10,

wherein said voltage supply unit generates said gate voltage which increases as said main current increases.

Claim 16 (Original): The drive circuit according to claim 10,

wherein said voltage supply unit controls said gate voltage to allow slowdown in switching speed of said transistor when said main current is lower than a certain level.